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## **ABSTRACT**

Methods and systems assess timing of PCI signals. A test mode is initiated within a host adapter board. A clock signal is generated for the host adapter board. PCI signals are generated within the host adapter board. One or more PCI signal lines of the host adapter board are electronically selected; and timing (e.g., slew rate and/or clock-to-signal valid) of the one or more PCI signal lines is assessed.